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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Application

Applicant(s): Roger Y. B. Young
Case: 03-0460
Serial No.: 10/628,614
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Art Unit: 2878
Examiner: Que Tan Le

Title: Wafer Edge Defect Inspection Using Captured Image Analysis

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APPEAL BRIEF

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313

Sir:

Applicant (hereinafter referred to as "Appellant") hereby appeals the final rejection, dated December 1, 2005, of claims 2-7 and 10-20 of the above referenced application.

REAL PARTY IN INTEREST

The present application is assigned of record to LSI Corporation, as evidenced by assignments in the U.S. Patent and Trademark Office at Reel 014338, Frame 0798, and at Reel 020548, Frame 0977. LSI Corporation is the real party in interest.

RELATED APPEALS AND INTERFERENCES

There are no known related appeals or interferences.

STATUS OF CLAIMS

The present application was filed on July 28, 2003 with claims 1-20. Claims 1, 8 and 9 have been canceled. Claims 2-7 and 10-20 remain pending. Claims 2, 4, 6, 7, 10, 13 and 16 are the pending independent claims.

Claims 4 and 16 stand rejected under 35 U.S.C. §102(e). Claims 2, 3, 5-7, 10-15 and 17-20 stand rejected under 35 U.S.C. §103(a). Claims 2-7 and 10-20 are appealed.

STATUS OF AMENDMENTS

There have no amendments filed subsequent to the outstanding final rejection.

SUMMARY OF CLAIMED SUBJECT MATTER

Independent claim 2 recites a method of inspecting a semiconductor wafer for defects using captured image analysis. The method comprises positioning the wafer with an edge thereof relative to a scanning electron microscope, rotating the wafer, scanning the edge of the rotating wafer with the scanning electron microscope, recording an image of the scanned wafer from the scanning electron microscope into a database, instructing a computer to analyze the recorded images of the scanned wafer, identifying any defects in the analyzed recorded images, and upon identifying any defects, recording defect information related to each defect.

An exemplary embodiment within the scope of claim 2 includes a method of inspecting a semiconductor wafer (e.g., 136 in FIGS. 3-8) for defects (e.g., 172-184 in FIG. 8) using captured image analysis. As described in the specification at, for example, page 10, line 24 to page 11, line 11, the method includes positioning the wafer with an edge thereof relative to a scanning electron microscope (e.g., 132, 134 in FIGS. 3-5). As described in the specification at, for example, page 10, lines 19-21, the method also includes rotating the wafer, and scanning the edge of the rotating wafer with the scanning electron microscope. As described in the specification at, for example, page 8, lines 19-20, and page 11, lines 21-23, the method further includes recording an image of the scanned wafer from the scanning electron microscope into a database (e.g., 126 in FIG. 2). As described in the specification at, for example, page 8, lines 27-30, the method also includes instructing a computer (e.g., 128 in

FIG. 2) to analyze the recorded images of the scanned wafer, and identifying any defects in the analyzed recorded images. As described in the specification at, for example, page 9, line 16 to page 10, line 2, and page 12, line 26 to page 13, line 2, the method further includes, upon identifying any defects, recording defect information related to each defect.

Independent claim 4 recites a method of inspecting a semiconductor wafer for defects using captured image analysis. The method includes a step of positioning the wafer with an edge thereof relative to an image capturing device. The method includes another step of positioning the image capturing device at a desired angle relative to the edge of the wafer. The method includes further steps of rotating the wafer and scanning the edge of the rotating wafer with the image capturing device. The method includes an additional step of recording an image of a desired portion of the edge of the scanned wafer from the image capturing device into a database. The method also includes instructing a computer to analyze the recorded images of the scanned wafer and identifying any defects in the analyzed recorded images. The method further includes, upon identifying any defects, recording defect information related to each defect.

An exemplary embodiment within the scope of claim 4 includes a method of inspecting a semiconductor wafer (e.g., 136 in FIGS. 3-8) for defects (e.g., 172-184 in FIG. 8) using captured image analysis. As described in the specification at, for example, page 10, line 24 to page 11, line 11, the method includes positioning the wafer with an edge thereof relative to an image capturing device (e.g., 132, 134 in FIGS. 3-5). As described in the specification at, for example, page 10, lines 19-21, the method also includes rotating the wafer, and scanning the edge of the rotating wafer with the image capturing device. As described in the specification at, for example, page 8, lines 19-20, and page 11, lines 21-23, the method further includes recording an image of a desired portion of the edge of the scanned wafer from the image capturing device into a database (e.g., 126 in FIG. 2). As described in the specification at, for example, page 8, lines 27-30, the method also includes instructing a computer (e.g., 128 in FIG. 2) to analyze the recorded images of the scanned wafer, and identifying any defects in the analyzed recorded images. As described in the specification at, for example, page 9, line 16 to page 10, line 2, and page 12, line 26 to page 13, line 2, the method further includes, upon identifying any defects, recording defect information related to each defect.

Independent claim 6 recites a method of inspecting a semiconductor wafer for defects using captured image analysis. The method includes performing the steps described in this paragraph after a first process step. The wafer is positioned with an edge thereof relative to an image capturing device. The wafer is rotated and the edge of the rotating wafer is scanned with the image capturing device. An image of the scanned wafer is recorded from the image capturing device into a database. A computer is instructed to analyze the recorded images of the scanned wafer, and any defects in the analyzed recorded images are identified. Upon identifying any defects, defect information related to each defect is recorded.

The method also includes repeating the aforementioned steps after a second process step. The method further includes comparing the defect information recorded after the first process step to the defect information recorded after the second process step. The method additionally includes identifying any new defects as added defects due to the second process step.

An exemplary embodiment within the scope of claim 6 includes a method of inspecting a semiconductor wafer (e.g., 136 in FIGS. 3-8) for defects (e.g., 172-184 in FIG. 8) using captured image analysis. As described in the specification at, for example, page 5, line 14, to page 6, line 19, with reference to FIG. 1, the method includes performing the steps described in this paragraph after a first process step (e.g., by Inspection System 2 at 118, following Fabrication Machine/Station 3 at 106). As described in the specification at, for example, page 10, line 24, to page 11, line 11, the wafer is positioned with an edge thereof relative to an image capturing device (e.g., 132, 134 in FIGS. 3-5). As described in the specification at, for example, page 10, lines 19-21, the wafer is rotated and the edge of the rotating wafer is scanned with the image capturing device. As described in the specification at, for example, page 8, lines 19-20, and page 11, lines 21-23, an image of the scanned wafer is recorded from the image capturing device into a database (e.g., 126 in FIG. 2). As described in the specification at, for example, page 8, lines 27-30, a computer (e.g., 128 in FIG. 2) is instructed to analyze the recorded images of the scanned wafer, and any defects in the analyzed recorded images are identified. As described in the specification at, for example, page 9, line 16, to page 10, line 2, and page 12, line 26, to page 13, line 2, upon identifying any defects, defect information related to each defect is recorded.

As described in the specification at, for example, page 5, line 14, to page 6, line 19, with reference to FIG. 1, the method also includes repeating the aforementioned steps after a second process step (e.g., by Inspection System 3 at 120, following Fabrication Machine/Station 6 at 112). As described in the specification at, for example, page 12, line 26, to page 13, line 2, the method further includes comparing defect information (e.g., 168 in FIG. 8) recorded after the first process step to the defect information (e.g., 170 in FIG. 8) recorded after the second process step. As described in the specification at, for example, page 13, lines 3-11, the method additionally includes identifying any new defects (e.g., defects 182 and 184) as added defects (e.g., 186 in FIG. 8) due to the second process step.

Independent claim 7 recites a method of inspecting a semiconductor wafer for defects using captured image analysis. The method includes performing the steps described in this paragraph after a first process step. The wafer is positioned with an edge thereof relative to an image capturing device. The wafer is rotated and the edge of the rotating wafer is scanned with the image capturing device. An image of the scanned wafer is recorded from the image capturing device into a database. A computer is instructed to analyze the recorded images of the scanned wafer, and any defects in the analyzed recorded images are identified. Upon identifying any defects, defect information related to each defect is recorded.

The method also includes repeating the aforementioned steps after a second process step. The method further includes comparing the defect information recorded after the first process step to the defect information recorded after the second process step. The method additionally includes determining whether any defects identified after the first process step have been reduced after the second process step, and identifying any such reduced defects as repaired defects.

An exemplary embodiment within the scope of claim 7 includes a method of inspecting a semiconductor wafer (e.g., 136 in FIGS. 3-8) for defects (e.g., 172-184 in FIG. 8) using captured image analysis. As described in the specification at, for example, page 5, line 14, to page 6, line 19, with reference to FIG. 1, the method includes performing the steps described in this paragraph after a first process step (e.g., by Inspection System 2 at 118, following Fabrication Machine/Station 3 at 106). As described in the specification at, for example, page 10, line 24, to page 11, line 11, the wafer is positioned with an edge thereof relative to an image capturing device (e.g., 132, 134 in FIGS. 3-5). As

described in the specification at, for example, page 10, lines 19-21, the wafer is rotated and the edge of the rotating wafer is scanned with the image capturing device. As described in the specification at, for example, page 8, lines 19-20, and page 11, lines 21-23, an image of the scanned wafer is recorded from the image capturing device into a database (e.g., 126 in FIG. 2). As described in the specification at, for example, page 8, lines 27-30, a computer (e.g., 128 in FIG. 2) is instructed to analyze the recorded images of the scanned wafer, and any defects in the analyzed recorded images are identified. As described in the specification at, for example, page 9, line 16, to page 10, line 2, and page 12, line 26, to page 13, line 2, upon identifying any defects, defect information related to each defect is recorded.

As described in the specification at, for example, page 5, line 14, to page 6, line 19, with reference to FIG. 1, the method also includes repeating the aforementioned steps after a second process step (e.g., by Inspection System 3 at 120, following Fabrication Machine/Station 6 at 112). As described in the specification at, for example, page 12, line 26, to page 13, line 2, the method further includes comparing the defect information (e.g., 168 in FIG. 8) recorded after the first process step to the defect information (e.g., 170 in FIG. 8) recorded after the second process step. As described in the specification at, for example, page 13, lines 11-14, the method additionally includes determining whether any defects identified after the first process step have been reduced after the second process step, and identifying any such reduced defects (e.g., 180 in FIG. 8) as repaired defects (e.g., 188 in FIG. 8).

Independent claim 10 recites a method of inspecting an edge of a semiconductor wafer for defects during fabrication of integrated circuit components on the semiconductor wafer within a fabrication system that includes a plurality of fabrication stations arranged in a processing order and within which a variety of process steps are performed on a plurality of wafers. The method includes a step of providing a plurality of inspection stations within the fabrication system corresponding to selected ones of the fabrication stations, wherein each inspection station is located in a subsequent processing order to a corresponding one of the selected fabrication stations.

The method also includes a step of processing a wafer in a first fabrication station. The method further includes automatically inspecting an edge of the wafer in a first inspection station. The method also includes automatically recording a first set of defects in the edge of the wafer. The method

additionally includes processing the wafer in a second fabrication station. The method further includes automatically recording a second set of defects in the edge of the wafer.

An illustrative embodiment within the scope of claim 10 includes a method of inspecting an edge of a semiconductor wafer (e.g., 136 in FIGS. 3-8) for defects (e.g., 172-184 in FIG. 8) during fabrication of integrated circuit components on the semiconductor wafer within a fabrication system (e.g., 100 in FIG. 1) that includes a plurality of fabrication stations (e.g., 102-114 in FIG. 1) arranged in a processing order and within which a variety of process steps are performed on a plurality of wafers, as described in the specification at, for example, page 5, lines 4-10. As described in the specification at, for example, page 5, line 10, to page 6, line 13, the method includes a step of providing a plurality of inspection stations (e.g., 116-122 in FIG. 1) within the fabrication system corresponding to selected ones (e.g., 104, 106/108, 112 and 114 in FIG. 1) of the fabrication stations, wherein each inspection station is located in a subsequent processing order to a corresponding one of the selected fabrication stations.

As described in the specification at, for example, page 5, lines 11-18, the method also includes a step of processing a wafer in a first fabrication station (e.g. 104 in FIGS. 1 and 2). As described in the specification at, for example, page 5, line 14, to page 6, line 19, the method further includes automatically inspecting an edge of the wafer in a first inspection station (e.g. 116 in FIGS. 1 and 2). As described in the specification at, for example, page 9, line 16, to page 10, line 2, and page 12, line 26, to page 13, line 2, the method also includes automatically recording a first set of defects (e.g., 168 in FIG. 8) in the edge of the wafer. As described in the specification at, for example, page 5, line 14, to page 6, line 19, the method additionally includes processing the wafer in a second fabrication station (e.g. 106 in FIGS. 1 and 2). As described in the specification at, for example, page 9, line 16 to page 10, line 2, and page 12, line 26 to page 13, line 2, the method further includes automatically recording a second set of defects (e.g., 170 in FIG. 8) in the edge of the wafer.

Independent claim 13 recites a method of inspecting an edge of semiconductor wafers for defects during fabrication of integrated circuit components on the semiconductor wafers within a fabrication system that includes a plurality of fabrication stations arranged in a processing order and within which a variety of process steps are performed on a plurality of wafers, as described in the

specification at. The method includes providing a plurality of inspection stations within the fabrication system corresponding to selected ones of the fabrication stations, wherein each inspection station is located in a subsequent processing order to a corresponding one of the selected fabrication stations.

The method also includes processing the wafers in the fabrication stations. The method further includes inspecting the edge of the wafers in the inspection stations. The method additionally includes, upon inspecting each wafer, recording an image of the edge of the wafer. The method further includes correlating each recorded image with the wafer from which it was taken and the process step after which it was taken.

An illustrative embodiment within the scope of claim 13 includes a method of inspecting an edge of semiconductor wafers (e.g., 136 in FIGS. 3-8) for defects (e.g., 172-184 in FIG. 8) during fabrication of integrated circuit components on the semiconductor wafers within a fabrication system (e.g., 100 in FIG. 1) that includes a plurality of fabrication stations (e.g., 102-114 in FIG. 1) arranged in a processing order and within which a variety of process steps are performed on a plurality of wafers, as described in the specification at, for example, page 5, lines 4-10. As described in the specification at, for example, page 5, line 10 to page 6, line 13, the method includes providing a plurality of inspection stations (e.g., 116-122 in FIG. 1) within the fabrication system corresponding to selected ones (e.g., 104, 106/108, 112 and 114 in FIG. 1) of the fabrication stations, wherein each inspection station is located in a subsequent processing order to a corresponding one of the selected fabrication stations.

As described in the specification at, for example, page 5, lines 11-18, the method also includes processing the wafers in the fabrication stations. As described in the specification at, for example, page 12, line 26 to page 13, line 14, the method further includes inspecting the edge of the wafers in the inspection stations. As described in the specification at, for example, page 8, lines 19-20, and page 11, lines 21-23, the method additionally includes, upon inspecting each wafer, recording an image of the edge of the wafer. As described in the specification at, for example, page 8, lines 20-25, the method further includes correlating each recorded image with the wafer from which it was taken and the process step after which it was taken.

Independent claim 16 recites a wafer edge defect inspection system. The wafer edge defect inspection system includes an image capturing device next to which a wafer can be positioned. The image capturing device is oriented to view at least a portion of an edge of the wafer. The image capturing device automatically generates an image of the edge of the wafer. The wafer edge defect system also includes a database connected to the image capturing device to receive the generated image of the edge of the wafer. The database automatically stores the received image for subsequent analysis. The wafer edge defect system additionally includes a computer connected to the database to retrieve the stored image upon instruction from a user to perform image analysis to locate any defects in the edge of the wafer.

An illustrative embodiment within the scope of claim 16 includes a wafer edge defect inspection system (e.g., 116 in FIGS. 1 and 2), as described in the specification at, for example, page 8, lines 4-6. As described in the specification at, for example, page 10, line 24, to page 11, line 11, the wafer edge defect inspection system includes an image capturing device (e.g., 132 and 134 in FIGS. 3-5) next to which a wafer (e.g., 136 in FIGS. 3-8) can be positioned. As described in the specification at, for example, page 12, lines 1-4, the image capturing device is oriented to view at least a portion of an edge of the wafer. As described in the specification at, for example, page 10, lines 19-21, the image capturing device automatically generates an image of the edge of the wafer. As described in the specification at, for example, page 8, lines 4-20, the wafer edge defect system also includes a database (e.g., 126 in FIG. 2) connected to the image capturing device to receive the generated image of the edge of the wafer. As described in the specification at, for example, page 9, lines 5-15, the database automatically stores the received image for subsequent analysis. As described in the specification at, for example, page 8, line 27, to page 9, line 8, the wafer edge defect system additionally includes a computer (e.g., 128 in FIG. 2) connected to the database to retrieve the stored image upon instruction from a user to perform image analysis to locate any defects in the edge of the wafer.

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

1. Claims 4 and 16 stand rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,906,794 (hereinafter "Tsuji").

2. Claims 2, 3, 5-7, 10-15 and 17-20 are rejected under 35 U.S.C. §103(a) as being unpatentable over Tsuji.

ARGUMENT

1. Rejection of claims 4 and 16 under 35 U.S.C. §102(e) over Tsuji

Claim 4

With regard to the §102 rejection of independent claim 4, Appellant initially notes that the Federal Circuit has recently reiterated that "unless a reference discloses within the four corners of the document not only all of the limitations claimed but also all of the limitations arranged or combined in the same way as recited in the claim, it cannot be said to prove prior invention of the thing claimed and, thus, cannot anticipate under 35 U.S.C. §102." *Net MoneyIN Inc. v. VeriSign Inc.*, 545 F.3d 1359, 1369, 88 USPQ2d 1751, 1760 (Fed. Cir. 2008)

Independent claim 4 includes a limitation directed to positioning the image capturing device at a desired angle relative to the edge of the wafer. In an illustrative embodiment described in the specification at, for example, page 12, lines 1-4, with reference to FIG. 7, image capturing device 134 may be moved relative to the edge 158 along the arrow A to any angle at which a desired portion of the edge is to be scanned.

In the Examiner's Answer dated November 1, 2007 (hereinafter "the Answer"), at page 7, first paragraph, the Examiner states that column 7 of Tsuji states that "the objective lens may be moved to the position located above the wafer edge portion." The Examiner further asserts that "the position located above the wafer edge portion is a desired angle relative to the edge of the wafer." Appellant respectfully asserts that the Examiner appears to be reading the relied-upon portion of Tsuji out of context. Tsuji, at column 7, lines 61-67, states (with the portion quoted by the Examiner underlined):

> [A]t the start of the edge observation, the 2-axis movement stage moves a semiconductor wafer in the X-Y plane perpendicular to the optical axis direction of the micro observation optical system, until the wafer edge portion comes to the

> position under the objective lens. Instead of this configuration, the objective lens may be moved to the position located above the wafer edge portion.

It is clear that the movement of the objective lens described in the cited portion is movement of the objective lens in an X-Y plane perpendicular to the semiconductor wafer until the objective lens is moved to a portion located above the wafer edge portion. Appellant respectfully submits that such movement will not change the angle of the objective lens relative to the edge of the wafer; rather, the objective lens will remain perpendicular to the semiconductor wafer. Accordingly, the cited portion of Tsuji fails to teach or even suggest the limitation at issue.

The Examiner also states in the Answer at page 7, first paragraph, that "in column 8, Tsuji discloses '(W)hen the imaging device is moved closer to the wafer 2'. Thus, the Tsuji reference does disclose the feature of 'positioning the image capturing device at a desired angle relative to the edge of the wafer' as claimed by the present application" (parenthesis and emphasis in original). Again, the Examiner appears to be reading the relied-upon portion of Tsuji out of context.

Specifically, Tsuji, at column 8, lines 51-52, states, with reference to FIG. 6, that "[w]hen the imaging device 74 is moved closer to the wafer 2, the scaling factor increases." However, increasing the scaling factor need not result in a change in the angle of imaging device 74 relative to wafer 2. See, for example, Tsuji at column 8, lines 35-40 ("The imaging device 74 is able to capture images at an arbitrary angle $\theta 2$ with respect to the wafer edge portion of the wafer 2. The scaling factor of the imaging device 74 can be arbitrarily determined, thereby enabling selection of an appropriate vertical resolution.")

In view of the above, one skilled in the art would reasonably interpret the described movement of the imaging device "closer to the wafer" such that "the scaling factor increases" to refer to movement along the axis defined by the solid black arrow pointed to by the label $\theta 2$, as shown in FIG. 6 of Tsuji. Such movement, however, will not affect the angle of imaging device 74 relative to wafer 2; the angle will remain at $\theta 2$.

Appellant further notes that the final Office Action dated December 1, 2005 (hereinafter "the final Office Action") at page 2, last paragraph, and the Answer at page 4, second paragraph, both

allege that "Tsuji's system inherently performs the claimed method steps." Appellant respectfully submits that, in "relying upon the theory of inherency, the examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied prior art." *Ex parte Levy,* 17 USPQ2d 1461, 1464 (Bd. Pat. App. & Inter. 1990) Moreover, the fact that a certain result or characteristic may occur or be present in the prior art is not sufficient to establish the inherency of that result or characteristic. See, e.g., *In re Rijckaert*, 9 F.3d 1531, 1534, 28 USPQ2d 1955, 1957 (Fed. Cir. 1993); *In re Oelrich*, 666 F.2d 578, 581-82, 212 USPQ 323, 326 (CCPA 1981). Rather, the evidence provided by the Examiner "must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill." *In re Robertson*, 169 F.3d 743, 745, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1999).

In view of the above, Tsuji clearly fails to disclose, either explicitly or inherently, the limitation of claim 4 directed to positioning the image capturing device at a desired angle relative to the edge of the wafer.

Claim 16

With regard to the §102 rejection of claim 16, Appellant again notes that the Federal Circuit has recently reiterated that "unless a reference discloses within the four corners of the document not only all of the limitations claimed but also all of the limitations arranged or combined in the same way as recited in the claim, it cannot be said to prove prior invention of the thing claimed and, thus, cannot anticipate under 35 U.S.C. §102." *Net MoneyIN Inc. v. VeriSign Inc.*, 545 F.3d 1359, 1369, 88 USPQ2d 1751, 1760 (Fed. Cir. 2008)

Independent claim 16 recites an arrangement which includes an image capturing device automatically generating an image of the edge of the wafer, and a database automatically storing the image for subsequent analysis. In an illustrative embodiment described in the present specification at, for example, page 12, lines 5-25, the image capturing device automatically scans

the desired portion of the edge of a wafer and captures an image thereof in accordance with a "recipe" that specifies various parameters that affect the image that will be captured.

Appellant respectfully submits that Tsuji does not teach or suggest these limitations. Instead, Tsuji appears to disclose that any edge inspection is manual, rather than automatic, since operator action is required to stop the rotation of the table 21 (Tsuji; FIG. 2) and capture an image of the desired portion of the wafer edge (see Tsuji at column 6, lines 1-9 - "The operator determines whether to rotate the wafer 2 or to stop it. . . .") and to end the observation of the wafer edge portion (see Tsuji at column 6, lines 24-26 - "When the operator determined to end the observation of the wafer edge portion in step S16, . . .").

The final Office Action at page 7, first paragraph, states that "Tsuji states that 'An automatic defect classification software is installed in the image processing section' while the image processing section is automatically performed." The Examiner apparently is referring to Tsuji, at column 6, lines 15-23. Appellant respectfully submits, however, that this automation refers to automatic classification of the defect, not to the automatic generating or storing of an image, as explicitly recited in claim 16.

The Examiner, in the Answer at page 7, last paragraph, characterizes arguments similar to the above as "an incorrect conclusion because the pointing device 50, at least as disclosed by Tsuji, is used to control the movement of the system's stage 30 and/or to control the rotation of the rotatable table 21 of the system but NOT for controlling the operation/performance of the image capturing device. (see columns 5-6 and figures 2-3). There is NO indication of whether or not the imaging device or camera 74 of Tsuji is operated directly by a user or operator."

Appellant respectfully disagrees. Tsuji clearly indicates that the imaging device captures an image when the operator manually depresses a rotation stop button. See Tsuji at column 5, lines 39-44 ("The rotatable table 21 keeps rotating until the operator depresses the rotation stop button. In response to the rotation of the rotatable table 21, the imaging device 100 captures an image of the edge portion of the wafer 2 located under the objective lens 60 and the display device displays the captured image.") and column 6, lines 4-8 ("When the operator finds an undesirable rinse cut amount or a defective portion such as a crack, the operator can depress the rotation stop

button to stop the rotation of the rotatable table 21 as the need arises. When the table 21 stops, an image of the wafer edge portion is captured by means of the imaging device 100 and image data obtained thereby is analyzed by means of the image processing section.")

More generally, FIG. 3 of Tsuji discloses a technique in which, before an image is captured by the imaging device, the operator must repeatedly and manually "confirm[] the image shown on the display device." See Tsuji at, for example, column 5, lines 22-23 (with reference to step S4); column 5, lines 29-30 (with reference to step S8); and column 6, lines 35-37 (with reference to step S20).

Tsuji clearly fails to teach or suggest automatically generating and storing an image, as recited in claim 16.

2. Rejection of claims 2, 3, 5-7, 10-15 and 17-20 under 35 USC §103(a) over Tsuji

Claim 2

Independent claim 2 includes limitations directed to positioning the wafer with an edge thereof relative to a scanning electron microscope, and scanning the edge of the rotating wafer with the scanning electron microscope. In formulating the rejection of claim 2 in the final Office Action at page 3, last paragraph, the Examiner argues that "although Tsuji fails to specify whether or not the microscope of the image capturing device including the use of a scanning electron microscope, the use of a scanning electron microscope for capturing image in an optical inspection system in order to provide better image information/data would have been known in the art."

As a preliminary matter, Appellant disputes the Examiner's contention that "Tsuji fails to specify whether or not the microscope of the image capturing device include[es] the use of a scanning electron microscope." As is known by one skilled in the art, "image magnification in the SEM is not a function of the power of the objective lens." Wikipedia, "Scanning Electron Microscope," §2.1, at http://en.wikipedia.org/wiki/Scanning_electron_microscope#Magnification (attached hereto as Exhibit 1). By contrast, Tsuji, at column 7, lines 39-42, states that "a small-magnification objective lens is replaced with a large-magnification objective lens so as to enable a defective portion to be displayed in an enlarged scale and examined in detail." See also Tsuji at column 6, lines 37-61, with reference

to FIGS. 4A and 4B. Thus, Tsuji clearly discloses an arrangement which does not use a scanning electron microscope. Indeed, the technique taught by Tsuji appears to be incompatible with the use of a scanning electron microscope, and hence Tsuji in fact teaches away therefrom.

Appellant respectfully notes that the Federal Circuit has held that an assessment of basic knowledge and common sense that is not based on any evidence in the record lacks "substantial evidence" support and may not form the basis for a rejection. *In re Zurko*, 258 F.3d 1379, 1385, 59 USPQ2d 1693, 1697 (Fed. Cir. 2001). Rather, the Examiner must provide specific factual findings predicated on sound technical and scientific reasoning to support his or her conclusion of common knowledge. See, e.g., *In re Soli*, 317 F.2d 941, 946, 137 USPQ 797, 801 (CCPA 1963); *In re Chevenard*, 139 F.2d 711, 713, 60 USPQ 239, 241 (CCPA 1943). Moreover, specific knowledge of the prior art must always be supported by citation to some reference work recognized as standard in the pertinent art. *In re Ahlert*, 424 F.2d 1088, 1091, 165 USPQ 418, 420-21 (CCPA 1970). The Examiner's conclusory assertion that the use of a scanning electron microscope would have been known in the art fails to satisfy this legal standard, and hence the Examiner has failed to present a proper *prima facie* obviousness rejection of claim 2.

Even if the Examiner could somehow establish that all aspects of the invention recited in claim 2 were individually known in the art, such arguments are insufficient to establish a *prima facie* case of obviousness. See, e.g., *KSR International Co. v. Teleflex Inc.*, 127 S.Ct. 1727, 1741, 82 USPQ2d 1385, 1396 (U.S. 2007) ("[A] patent composed of several elements is not proved obvious merely by demonstrating that each of its elements was, independently, known in the prior art.") Rather, the Examiner must provide an explicit "reason to combine the known elements in the fashion claimed by the patent at issue." *Id.*

Here, the Examiner argues that, because "the use of a scanning electron microscope for capturing image [sic] in an optical inspection system in order to provide better image information/data would have been known in the art," it "would have been obvious to one of ordinary skill in the art at the time of the invention to modify Tsuji accordingly in order to provide more accurate inspection results from the system." (Final Office Action; page 3, last paragraph)

Appellant respectfully submits that the proffered motivation appears to be a conclusory statement of the type ruled legally insufficient by the both Supreme Court and the Federal Circuit, particularly in view of the aforementioned failure of the Examiner to provide any support for the assertion that it was known in the art that the use of a scanning electron microscope would have provided better image information. See *KSR*, 127 S.Ct. at 1741, 82 USPQ2d at 1396, quoting *In re Kahn*, 441 F. 3d 977, 988, 78 USPQ2d 1329, 1336 (Fed. Cir. 2006) ("[R]ejections on obviousness grounds cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness.").

Thus, even assuming that it were possible to have modified Tsuji to reach the limitations of claim 2, the Examiner's proffered motivation for doing so is deficient, especially in view of the explicit teaching away found in the Tsuji reference. As recently noted by the Supreme Court, "when the prior art teaches away from combining certain known elements, discovery of a successful means of combining them is more likely to be nonobvious." *KSR*, 82 USPQ2d at 1395 (citing *United States* v. *Adams*, 383 U.S. 39, 51-52, 148 USPQ 479, 484 (1966)).

<u>Claim 3</u>

Claim 3 is believed to be patentable over Tsuji at least by virtue of its dependency from independent claim 2, the patentability of which is discussed above. Moreover, claim 3 is believed to define additional, separately-patentable subject matter.

Dependent claim 3 recites a limitation directed to setting an angle of the image capturing device relative to the edge of the wafer. Appellant respectfully notes that the final Office Action does not discuss this limitation in formulating the rejection of claim 3 at page 3, last paragraph. This deficiency is not remedied in the Answer at, for example, page 5, second paragraph. As discussed above with reference to independent claim 4, Tsuji fails to teach or suggest any arrangement which teaches or suggests this limitation of claim 3 involving setting an angle of the image capturing device relative to the edge of the wafer.

Moreover, Appellant respectfully submits that Tsuji fails to teach or suggest another limitation of claim 3 relating to an arrangement in which a "brightness of an illumination source

that illuminates the edge of the wafer" is set. The Examiner has also failed to discuss this limitation in the final Office Action at page 3, last paragraph or in the Answer at page 5, second paragraph. Accordingly, the rejection of claim 3 is both substantively and procedurally deficient.

Appellant notes that dependent claim 3 also includes a limitation directed to setting "an accelerating voltage of an electron beam." In both the final Office Action at page 3, last paragraph, and in the Answer at page 5, second paragraph, the Examiner merely asserts that the "further inclusion of setting an accelerating voltage of an electron beam would have also been obvious for similar reasons set forth above" with regard to claim 2. Appellant respectfully submits that this statement suffers from at least the deficiencies discussed above with reference to claim 2. Indeed, the conclusory statement which the Examiner attempts to incorporate by reference is even more deficient when applied to claim 3 than to claim 2, as such statement at least purports to address the limitations of claim 2.

Claim 5

Claim 5 is believed to be patentable over Tsuji at least by virtue of its dependency from independent claim 4, the patentability of which is discussed above. Claim 5 is also believed to define additional, separately-patentable subject matter. More particularly, claim 5 includes a limitation directed to scanning the edge of the wafer from a region interior of a top of the edge to a region exterior of a bottom of the edge.

In formulating the rejection of claim 5 in the final Office Action at page 4, first paragraph, and in the Answer at page 5, third paragraph, the Examiner concedes that Tsuji fails to disclose the limitations of claim 5. Rather, the Examiner asserts that "selecting a specific manner for scanning an object to be inspected or a wafer for providing a specific pattern of image to be taken by the image capturing device would have been obvious to one of ordinary skill in the art. It would have been obvious to modify Tsuji accordingly in order to provide a better image pattern to be recorded or stored or displayed."

Appellant initially notes that Tsuji discloses a technique wherein the specific portion of the wafer edge to be observed is selected manually by an operator using a pointing device. See Tsuji

at, for example, column 4, line 41, to column 5, line 61. There is no teaching or suggestion in Tsuji directed to selecting any manner for scanning an object to be inspected or providing a specific pattern of images to be taken by an image capturing device; rather, these selections must be made manually by the operator.

Moreover, Appellant respectfully submits that the proffered motivation appears to be a conclusory statement of the type ruled legally insufficient by the both Supreme Court and the Federal Circuit, particularly in view of the failure of the Examiner to provide any support for the assertion that it was known in the art that the specific pattern recited in claim 5 would have been known to one skilled in the art. Thus, claim 5 suffers from deficiencies of a type similar to those identified above with reference to dependent claim 2.

Claim 6

Independent claim 6 recites limitations directed to comparing the defect information recorded after the first process step to the defect information recorded after the second process step, and identifying any new defects as added defects due to the second process step. In illustrative embodiments described in the specification at, for example, page 5, line 27, to page 6, line 14; page 9, line 22, to page 10, line 2; and page 12, line 26, to page 13, line 14, comparison of "before" and "after" data for a given wafer advantageously allows for determination of whether a given process step has added defects to that wafer.

In formulating the rejection of claim 6 in the final Office Action at page 4, second paragraph, the Examiner concedes that "Tsuji lacks a clear inclusion of comparing the previous defect information to the after defect information to located any added defects." However, the Examiner alleges that "repeatedly inspecting the same area or portion of an inspected object or wafer for ensuring a complete inspection would have been obvious to one of ordinary skill in the inspection art." *Id.*

Appellant respectfully submits that Tsuji does in fact teach a technique in which a wafer is repeatedly inspected but which still fails to teach or suggest the limitations of claim 6. Tsuji, at column 1, lines 52-62, indicates that "defect inspection is carried out in each manufacturing step,"

however, it teaches that in such "defect inspection, the surface of the semiconductor wafer is mainly inspected to see if there are scratches, dust, cracks, stains, or uneven portions," and that this is done in "as early a step as possible to determine whether the wafer is good or bad."

Tsuji at column 8, lines 54-56, states that the "edge defect processing section 75 compares the belt-like image data acquired by the imaging device 74 with image data on a wafer of good quality." More specifically, Tsuji at column 9, lines 6-13, clearly indicates that the "image data on the semiconductor wafer 2 of good quality . . . is belt-like image data obtained with respect to a wafer 2 which is considered to be a good one in previous inspection. Alternatively, the wafers 2 of one lot are sequentially inspected, and each time a wafer 2 of good quality is determined, the image data of that wafer 2 is used as updating data."

As such, Tsuji at most suggests a technique in which, after each manufacturing step, image data acquired by an imaging device is compared with image data on a wafer of good quality. It is important to note that this "image data on a wafer of good quality" is <u>not</u> previous image data from the wafer being inspected, but rather is a <u>different</u> wafer (a wafer of known good quality) which has been previously inspected. In other words, rather than comparing defect information recorded for a wafer after the first process step to the defect information recorded for that wafer after the second process step, Tsuji compares information recorded for a wafer after a given process step with information recorded for a previously-inspected different "wafer of good quality."

Thus, rather than teaching or suggesting the arrangement recited in claim 6, Tsuji instead discloses a "conventional image-analysis technique" described in the specification at, for example, page 9, lines 16-21, in which "the recorded image of the edge of a selected wafer is preferably compared to an image of an ideal wafer edge to generate defect data indicating the locations of possible defects on the edge of the selected wafer."

In view of the foregoing, Appellant respectfully submits that Tsuji fails to teach or suggest the limitations of claim 6 directed to comparing the defect information recorded after the first process step to the defect information recorded after the second process step, and identifying any new defects as added defects due to the second process step.

Claim 7

Independent claim 7 recites limitations directed to comparing the defect information recorded after the first process step to the defect information recorded after the second process step, determining whether any defects identified after the first process step have been reduced after the second process step, and identifying any such reduced defects as repaired defects.. In illustrative embodiments described in the specification at, for example, page 5, line 27, to page 6, line 14; page 9, line 22, to page 10, line 2; and page 12, line 26, to page 13, line 14, comparison of "before" and "after" data for a given wafer advantageously allows for determination of whether a given process step has repaired defects in that wafer.

In formulating the rejection of claim 7 in the final Office Action at page 4, second paragraph, the Examiner concedes that "Tsuji lacks a clear inclusion of comparing the previous defect information to the after defect information to locate any . . . repaired defects." However, the Examiner alleges that "repeatedly inspecting the same area or portion of an inspected object or wafer for ensuring a complete inspection would have been obvious to one of ordinary skill in the inspection art." *Id.*

Appellant respectfully submits that Tsuji does in fact teach a technique in which a wafer is repeatedly inspected but which still fails to teach or suggest the limitations of claim 7. Specifically, Tsuji, at column 1, lines 52-62, indicates that "defect inspection is carried out in each manufacturing step," however, it teaches that in such "defect inspection, the surface of the semiconductor wafer is mainly inspected to see if there are scratches, dust, cracks, stains, or even portions," and that this is done so as to "as early a step as possible to determine whether the wafer is good or bad."

Tsuji at column 8, lines 54-56, states that the "edge defect processing section 75 compares the belt-like image data acquired by the imaging device 74 with image data on a wafer of good quality." More specifically, Tsuji at column 9, lines 6-13, clearly indicates that the "image data on the semiconductor wafer 2 of good quality . . . is belt-like image data obtained with respect to a wafer 2 which is considered to be a good one in previous inspection. Alternatively, the wafers 2

of one lot are sequentially inspected, and each time a wafer 2 of good quality is determined, the image data of that wafer 2 is used as updating data."

As such, Tsuji at most suggests a technique in which, after each manufacturing step, image data acquired by an imaging device is compared with image data on a wafer of good quality. It is important to note that this "image data on a wafer of good quality" is not previous image data from the wafer being inspected, but rather is a different wafer which has been previously inspected. In other words, rather than comparing defect information recorded for a wafer after the first process step to the defect information recorded for that wafer after the second process step, Tsuji compares information recorded for a wafer after a given process step with information recorded for a previously-inspected "wafer of good quality."

Thus, rather than teaching or suggesting the arrangement recited in claim 6. Tsuji instead discloses a "conventional image-analysis technique" described in the specification at, for example, page 9, lines 16-21, in which "the recorded image of the edge of a selected wafer is preferably compared to an image of an ideal wafer edge to generate defect data indicating the locations of possible defects on the edge of the selected wafer."

Moreover, in the arrangement taught by Tsuji, the wafer being inspected is compared with a "wafer of good quality." By definition, a wafer of good quality will not have defects. As such, the data with which the wafer being inspected is compared in Tsuji will not have any identified defects, thus making it impossible to determine whether any defects identified after a first process step have been reduced after a second process step, and hence whether any defects have been repaired.

In view of the foregoing, Appellant respectfully submits that Tsuji fails to teach or suggest the limitations of claim 7 directed to comparing the defect information recorded after the first process step to the defect information recorded after the second process step, determining whether any defects identified after the first process step have been reduced after the second process step, and identifying any such defects as repaired defects.

Claim 10

Independent claim 10 recites automatically inspecting an edge of the wafer in a first inspection station, automatically recording a first set of defects in the edge of the wafer, automatically inspecting the edge of the wafer in a second inspection station, and automatically recording a second set of defects in the edge of the wafer.

As discussed above with reference to independent claim 4, Tsuji fails to teach or suggest any automatic inspection of an edge of a wafer and automatic recording of a set of defects in the edge of a wafer. Thus, Tsuji clearly fails to teach or suggest the limitations recited in independent claim 16 directed to automatically inspecting an edge of the wafer in a first inspection station, automatically recording a first set of defects in the edge of the wafer, automatically inspecting the edge of the wafer in a second inspection station, and automatically recording a second set of defects in the edge of the wafer.

Claims 11 and 12

Claim 11 is believed to be patentable over Tsuji at least by virtue of its dependency from independent claim 10, the patentability of which is discussed above. Claim 11 is also believed to define additional, separately-patentable subject matter. Dependent claim 11 recites determining a difference between the first and second sets of defects.

As discussed above with regard to independent claims 6 and 7, rather than comparing defect information recorded for a wafer after the first process step to the defect information recorded for that wafer after the second process step, Tsuji compares information recorded for a wafer after a given process step with information recorded for a previously-inspected "wafer of good quality." Thus, Tsuji clearly fails to teach or suggest determining a difference between first and second sets of deficits in the edge of a given wafer, as recited in claim 11.

Dependent claim 12 is believed to be patentable over Tsuji at least by virtue of its dependency from independent claim 10 and dependent claim 11, the patentability of which are discussed above.

Claims 13 and 14

Independent claim 13 includes a limitation directed to correlating each recorded image with the wafer from which it was taken and the process step after which it was taken. The final Office Action at page 6, second paragraph, lists several types of information that Tsuji may disclose as being stored, but none of this information is related to the process step after which a recorded image is taken, as claimed in claim 13. Tsuji discloses only that image data, related defect data, "the coordinates and the rotating angle of a portion [of the wafer] being observed," and a wafer identification number may be correlated. See Tsuji at, for example, column 6, lines 62-65; column 7, lines 1-6 and 54-56; column 11, lines 34-42. Tsuji does not teach or suggest, however, that this information is correlated with the process step after which the recorded image was taken, and hence fails to teach or suggest the limitations of independent claim 13.

Claim 14 is believed to be patentable over Tsuji at least by virtue of its dependency from independent claim 13, the patentability of which is discussed above.

Claim 15

Claim 15 is believed to be patentable over Tsuji at least by virtue of its dependency from independent claim 13, the patentability of which is discussed above. Claim 15 is also believed to define additional, separately-patentable subject matter. More particularly, claim 15 recites limitations directed to selecting two recorded images by specifying the wafer from which both images were taken and the two process steps after which each selected image was taken, determining any defects that were present on the edge of the specified wafer at times that the two selected recorded images were taken of the edge of the specified wafer by analyzing the two selected recorded images, and determining whether any defects were added to the edge of the specified wafer.

Appellant respectfully submits that Tsuji does not teach or suggest these limitations. As discussed above with reference to independent claim 6, rather than comparing defect information recorded for a wafer after a first process step to the defect information recorded for that wafer after a second process step, Tsuji compares information recorded for a wafer after a given process step with information recorded for a "wafer of good quality," which is a different wafer.

Accordingly, there is no analysis of two selected recorded images of the same specified wafer, much less any determination of whether any defects were added to the specified wafer based on such analysis.

Claims 17 and 18

Claim 17 is believed to be patentable over Tsuji at least by virtue of its dependency from independent claim 16, the patentability of which is discussed above. Claim 17 is also believed to define additional, separately-patentable subject matter. More particularly, claim 17 includes limitations wherein a first image capturing device generates the first image of the edge of the wafer after the first process step, a second image capturing device generates a second image of the edge of the wafer after the second process step, and a computer retrieves the stored first and second images upon instruction from the user to compare and analyze the first and second images together.

As discussed above with reference to claim 6, rather than analyzing an image of a wafer after a first process step with an image of that wafer after the second process step, as recited in dependent claim 17, Tsuji compares an image recorded for a wafer after a given process step with an image recorded for a previously-inspected "wafer of good quality."

Claim 18 is believed to be patentable over Tsuji at least by virtue of its dependency from independent claim 17, the patentability of which is discussed above.

Claim 19

Claim 19 is believed to be patentable over Tsuji at least by virtue of its dependency from independent claim 17, the patentability of which is discussed above. Claim 19 is also believed to define additional, separately-patentable subject matter. More particularly, claim 19 recites limitations wherein the computer compares and analyzes the first and second images together to determine whether any defects have been repaired on the edge of the wafer between times that the first and second images thereof are generated.

As discussed above with reference to independent claim 7, the data with which the wafer being inspected is compared in Tsuji will not have any identified defects, thus making it

impossible to determine whether any defects identified after a first process step have been reduced after a second process step, and hence whether any defects have been repaired.

Claim 20

Claim 17 is believed to be patentable over Tsuji at least by virtue of its dependency from independent claim 16, the patentability of which is discussed above.

In view of the above, Appellant believes that claims 2-7 and 10-20 are in condition for allowance, and respectfully requests reversal of the present rejections.

Respectfully submitted,

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CLAIMS APPENDIX

1. (Canceled)

2. A method of inspecting a semiconductor wafer for defects using captured image analysis comprising:

positioning the wafer with an edge thereof relative to a scanning electron microscope;

rotating the wafer;

scanning the edge of the rotating wafer with the scanning electron microscope;

recording an image of the scanned wafer from the scanning electron microscope into a database;

instructing a computer to analyze the recorded images of the scanned wafer;

identifying any defects in the analyzed recorded images; and

upon identifying any defects, recording defect information related to each defect.

3. A method as defined in claim 2 further comprising:

before scanning the edge of the wafer, setting an angle of the image capturing device relative to the edge of the wafer, a brightness of an illumination source that illuminates the edge of the wafer, and an accelerating voltage of an electron beam.

4. A method of inspecting a semiconductor wafer for defects using captured image analysis comprising:

positioning the wafer with an edge thereof relative to an image capturing device;

positioning the image capturing device at a desired angle relative to the edge of the wafer;

rotating the wafer;

scanning the edge of the rotating wafer with the image capturing device;

recording an image of a desired portion of the edge of the scanned wafer from the image capturing device into a database;

instructing a computer to analyze the recorded images of the scanned wafer;

identifying any defects in the analyzed recorded images; and

upon identifying any defects, recording defect information related to each defect.

5. A method as defined in claim 4 wherein:

the scanning step further comprises:

scanning the edge of the wafer from a region interior of a top of the edge to a region exterior of a bottom of the edge.

6. A method of inspecting a semiconductor wafer for defects using captured image analysis comprising:

after a first process step:

positioning the wafer with an edge thereof relative to an image capturing device;

rotating the wafer;

scanning the edge of the rotating wafer with the image capturing device;

recording an image of the scanned wafer from the image capturing device into a database;

instructing a computer to analyze the recorded images of the scanned wafer;

identifying any defects in the analyzed recorded images; and

upon identifying any defects, recording defect information related to each defect;

after a second process step, repeating the aforementioned steps;

comparing the defect information recorded after the first process step to the defect information recorded after the second process step; and

identifying any new defects as added defects due to the second process step.

7. A method of inspecting a semiconductor wafer for defects using captured image analysis comprising:

after a first process step:

positioning the wafer with an edge thereof relative to an image capturing device;

rotating the wafer;

scanning the edge of the rotating wafer with the image capturing device;

recording an image of the scanned wafer from the image capturing device into a database;

instructing a computer to analyze the recorded images of the scanned wafer,

identifying any defects in the analyzed recorded images; and

upon identifying any defects, recording defect information related to each defect;

after a second process step, repeating the aforementioned steps;

comparing the defect information recorded after the first process step to the defect information recorded after the second process step;

determining whether any defects identified after the first process step have been reduced after the second process step; and

identifying any such reduced defects as repaired defects.

8. (Canceled)

9. (Canceled)

10. A method of inspecting an edge of a semiconductor wafer for defects during fabrication of integrated circuit components on the semiconductor wafer within a fabrication system that includes a plurality of fabrication stations arranged in a processing order and within which a variety of process steps are performed on a plurality of wafers, comprising:

providing a plurality of inspection stations within the fabrication system corresponding to selected ones of the fabrication stations, each inspection station being located in a subsequent processing order to a corresponding one of the selected fabrication stations;

processing a wafer in a first fabrication station;

automatically inspecting an edge of the wafer in a first inspection station;

automatically recording a first set of defects in the edge of the wafer; processing the wafer in a second fabrication station;

automatically inspecting the edge of the wafer in a second inspection station; and

automatically recording a second set of defects in the edge of the wafer.

11. A method as defined in claim 10 further comprising:

determining a difference between the first and second sets of defects.

12. A method as defined in claim 11 further comprising:

identifying process-induced edge defects from the determined difference between the first and second sets of defects.

13. A method of inspecting an edge of semiconductor wafers for defects during fabrication of integrated circuit components on the semiconductor wafers within a fabrication system that includes a plurality of fabrication stations arranged in a processing order and within which a variety of process steps are performed on a plurality of wafers, comprising:

providing a plurality of inspection stations within the fabrication system corresponding to selected ones of the fabrication stations, each inspection station being located in a subsequent processing order to a corresponding one of the selected fabrication stations;

processing the wafers in the fabrication stations;

inspecting the edge of the wafers in the inspection stations;

upon inspecting each wafer, recording an image of the edge of the wafer; and

correlating each recorded image with the wafer from which it was taken and the process step after which it was taken.

14. A method as defined in claim 13 further comprising:

selecting a recorded image from among a plurality of the recorded images by specifying the wafer from which it was taken and the process step after which it was taken; and

determining whether any defects were present on the edge of the specified wafer at a time that the selected recorded image was taken of the edge of the specified wafer by analyzing the selected recorded image.

15. A method as defined in claim 13 further comprising:

selecting two recorded images from among a plurality of the recorded images by specifying the wafer from which both images were taken and the two process steps after which each selected image was taken;

determining any defects that were present on the edge of the specified wafer at times that the two selected recorded images were taken of the edge of the specified wafer by analyzing the two selected recorded images; and

determining whether any defects were added to the edge of the specified wafer between the times that the two selected recorded images were taken by comparing the determined defects from the analyzing of the two selected recorded images.

16. A wafer edge defect inspection system comprising:

an image capturing device next to which a wafer can be positioned, the image capturing device being oriented to view at least a portion of an edge of the wafer, the image capturing device automatically generating an image of the edge of the wafer;

a database connected to the image capturing device to receive the generated image of the edge of the wafer, the database automatically storing the received image for subsequent analysis; and

a computer connected to the database to retrieve the stored image upon instruction from a user to perform image analysis to locate any defects in the edge of the wafer.

17. A wafer edge defect inspection system as defined in claim 16, wherein the image capturing device is a first image capturing device, the image generated thereby is a first image and the wafer edge defect inspection system is incorporated into a fabrication system having a plurality of fabrication stations for processing the wafer and forming integrated circuit components thereon, further comprising:

a second image capturing device next to which the wafer can be positioned, the second image capturing device being oriented to view at least the portion of the edge of the wafer, the second image capturing device automatically generating a second image of the edge of the wafer and being connected to the database to supply the second image to the database;

and wherein:

the database automatically stores the second image for subsequent analysis by the computer;

the first image capturing device is incorporated into the fabrication system to receive the wafer after a first fabrication station performs a first process step on the wafer and the first image capturing device generates the first image of the edge of the wafer after the first process step;

the second image capturing device is incorporated into the fabrication system to receive the wafer after a second fabrication station performs a second process step on the-wafer and the second image capturing device generates the second image of the edge of the wafer after the second process step; and

the computer retrieves the stored first and second images upon instruction from the user to compare and analyze the first and second images together.

18. A wafer edge defect inspection system as defined in claim 17, wherein:

the computer compares and analyzes the first and second images together upon instruction from the user to determine whether any defects have been added to the edge of the wafer between times that the first and second images thereof are generated.

19. A wafer edge defect inspection system as defined in claim 17, wherein:

the computer compares and analyzes the first and second images together upon instruction from the user to determine whether any defects have been repaired on the edge of the wafer between times that the first and second images thereof are generated.

20. A wafer edge defect inspection system as defined in claim 16 incorporated into a fabrication system having a plurality of fabrication stations within which the wafer is subjected to process steps to form integrated circuit components thereon, and wherein:

at least a portion of the located defects are caused by at least one of the process steps to which the wafer is subjected before the image capturing device automatically generates the image of the edge of the wafer.

EVIDENCE APPENDIX

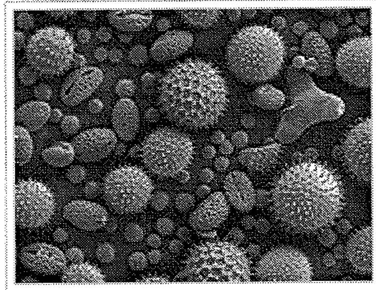
Submitted herewith as Exhibit 1 is a printout of the relevant portion of Wikipedia, "Scanning Electron Microscope," §2.1, as available at http://en.wikipedia.org/wiki/Scanning_electron_microscope#Magnification.

EXHIBIT 1

Scanning electron microscope

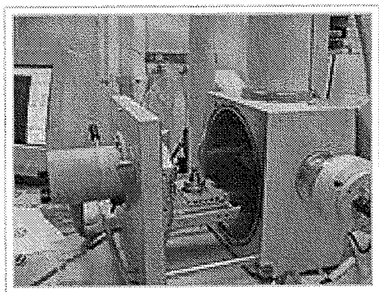
From Wikipedia, the free encyclopedia

The **scanning electron microscope** (**SEM**) is a type of electron microscope that images the sample surface by scanning it with a high-energy beam of electrons in a raster scan pattern. The electrons interact with the atoms that make up the sample producing signals that contain information about the sample's surface topography, composition and other properties such as electrical conductivity.



These pollen grains taken on an SEM show the characteristic depth of field of SEM micrographs.

SEM *Cambridge S150* with EDAX (left) at Kiel University (1980)



SEM opened sample chamber

The types of signals produced by an SEM include secondary electrons, back scattered electrons (BSE), characteristic x-rays, light (cathodoluminescence), specimen current and transmitted electrons. These types of signal all require specialized detectors for their detection that are not usually all present on a single machine. The signals result from interactions of the electron beam with atoms at or near the surface of the sample. In the most common or standard detection mode, secondary electron imaging or SEI, the SEM can produce very high-resolution images of a sample surface, revealing details about 1 to 5 nm in size. Due to the way these images are created, SEM micrographs have a very large depth of field yielding a characteristic three-dimensional appearance useful for understanding the surface structure of a sample. This is exemplified by the micrograph of pollen shown to the right. A wide range of magnifications is possible, from about x 25 (about equivalent to that of a powerful hand-lens) to about x 250,000, about 250 times the magnification limit of the best light microscopes. Back-scattered electrons (BSE) are beam electrons that are reflected from the sample by elastic scattering. BSE are often used in analytical SEM along with the spectra made from the characteristic x-rays. Because the intensity of the BSE signal is strongly related to the atomic number (Z) of the specimen, BSE images can provide information about the distribution of different elements in the sample. For the same reason BSE imaging can image colloidal gold immuno-labels of 5 or 10 nm diameter, that would otherwise be difficult or impossible to detect in secondary electron images in biological specimens. Characteristic X-rays are emitted when the electron beam removes an inner shell electron from the sample, causing a higher energy electron to fill the shell and release energy. These characteristic x-rays are used to identify the composition and measure the abundance of elements in the sample.

Contents

History

The first SEM image was obtained by Max Knoll, who in 1935 obtained an image of silicon steel showing electron channeling contrast.[1] Further pioneering work on the physical principles of the SEM and beam specimen interactions was performed by Manfred von Ardenne in 1937,[2][3] who produced a British patent[4] but never made a practical instrument. The SEM was further developed by Professor Sir Charles Oatley and his postgraduate student Gary Stewart and was first marketed in 1965 by the Cambridge Instrument Company as the "Stereoscan". The first instrument was delivered to DuPont.

Scanning process and image formation

In a typical SEM, an electron beam is thermionically emitted from an electron gun fitted with a tungsten filament cathode. Tungsten is normally used in thermionic electron guns because it has the highest melting point and lowest vapour pressure of all metals, thereby allowing it to be heated for electron emission, and because of its low cost. Other types of electron emitters include lanthanum hexaboride (LaB_6) cathodes, which can be used in a standard tungsten filament SEM if the vacuum system is upgraded and field emission guns (FEG), which may be of the cold-cathode type using tungsten single crystal emitters or the thermally-assisted Schottky type, using emitters of zirconium oxide.

The electron beam, which typically has an energy ranging from a few hundred eV to 40 keV, is focused by one or two condenser lenses to a spot about 0.4 nm to 5 nm in diameter. The beam passes through pairs of scanning coils or pairs of deflector plates in the electron column, typically in the final lens, which deflect the beam in the x and y axes so that it scans in a raster fashion over a rectangular area of the sample surface.

When the primary electron beam interacts with the sample, the electrons lose energy by repeated random scattering and absorption within a teardrop-shaped volume of the specimen known as the interaction volume, which extends from less than 100 nm to around 5 µm into the surface. The size of the interaction volume depends on the electron's landing energy, the atomic number of the specimen and the specimen's density. The energy exchange between the electron beam and the sample results in the reflection of high-energy electrons by elastic scattering, emission of secondary electrons by inelastic scattering and the emission of electromagnetic radiation, each of which can be detected by specialized detectors. The beam current absorbed by the specimen can also be detected and used to create images of the distribution of specimen current. Electronic amplifiers of various types are used to amplify the signals which are displayed as variations in brightness on a cathode ray tube. The raster scanning of the CRT display is synchronised with that of the beam on the specimen in the microscope, and the resulting image is therefore a distribution map of the intensity of the signal being emitted from the scanned area of the specimen. The image may be captured by photography from a high resolution cathode ray tube, but in modern machines is digitally captured and displayed on a computer monitor and saved to a computer's hard disc.

Magnification

Magnification in a SEM can be controlled over a range of up to 6 orders of magnitude from about x25 to x 250,000 and exceptionally to 2 million times in the Hitachi S-5500 in-lens Field Emission SEM, imaging a specimen area about 60nm wide with resolution up to 0.4 nm. Unlike optical and transmission electron microscopes, image magnification in the SEM is not a function of the power of the objective lens. SEMs may have condenser and objective lenses, but their function is to focus the beam to a spot, and not to image the specimen. Provided the electron gun can generate a beam with sufficiently small diameter, an SEM could in principle work entirely without condenser or objective lenses, although it might not be very versatile or achieve very high resolution. In an SEM, as in scanning probe microscopy, magnification results from the ratio of the dimensions of the raster on the specimen and the raster on the display device. Assuming that the display screen has a fixed size, higher magnification results from reducing the size of the raster on the specimen, and vice versa. Magnification is therefore controlled by the current supplied to the x,y scanning coils, and not by objective lens power.

RELATED PROCEEDINGS APPENDIX

None.